REMARKS

The Final Office Action mailed September 26, 2001, has been received and reviewed. Claims 1 through 28 and 100 through 129 are currently pending in the application. Claims 1 through 28 and 100 through 129 stand rejected. Applicant proposes to amend claims 1, 8, 9, 12, 16, 102, 108, 109, 112 and 116, and respectfully requests reconsideration of the application as proposed to be amended herein.

35 U.S.C. § 102 Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 6,277,745 to Liu et al.

Claims 1, 4 through 8, 10 through 13, and 15 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Lui et al (U.S. Patent No. 6,277,745). Applicant respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Liu discloses a passivation method of post copper dry etching. Liu discloses a sandwich structure consisting of a bottom barrier layer, a copper layer and a top barrier layer. After formation of this sandwich structure and patterning, the exposed sidewalls are passivated by means of a barrier metal spacer process. Liu teaches that the fully encapsulated copper lines are highly resistant to oxidation which is an otherwise inherent problem with bare copper lines.

By way of contrast, independent claim 1, as proposed to be amended, recites a metallization structure for a semiconductor device, comprising a substrate comprising a substantially planar upper surface; and a conductive line for transmitting a signal laterally across said substrate, said conductive line comprising a metal layer defining a pattern on a portion of the substrate upper surface; a single conducting layer overlying and substantially coextensive with the metal layer, said metal layer and

said single conducting layer having substantially aligned sidewalls and an upper surface out of contact with any metal; and metal spacers flanking the sidewalls of the single conducting layer and metal layer.

Applicant respectfully submits that Liu fails to teach a single conducting layer having substantially aligned sidewalls and an upper surface out of contact with any metal. Instead, Liu teaches that a novel aspect of its invention are the fully encapsulated copper lines that are highly resistant to oxidation which is an otherwise inherent problem with bare copper lines. (Liu, abstract). Applicant notes that caps, such the top barrier layer in Liu, are known in the prior art. (Specification, page 4, lines 10-14). However, in claim 1, as proposed to be amended, the upper surface of the single conducting layer is out of contact with any metal. As Liu fails to teach every limitation of independent claim 1, as proposed to be amended, applicant respectfully submits that Liu does not anticipate claim 1. Thus, claim 1 is allowable.

Claims 2 through 15 and 100 are each allowable as depending, either directly or indirectly, from allowable claim 1.

Claim 2 is further allowable as Liu fails to teach a dielectric layer on the substrate upper surface and underlying the metal layer.

Claim 3 is further allowable as Liu fails to teach the dielectric layer is silicon oxide or BPSG.

Claim 9 is further allowable as Liu fails to teach the single conducting layer is an aluminum-copper alloy.

Claim 12 is further allowable as Liu fails to teach a dielectric layer on the single conducting layer and having sidewalls aligned with said sidewalls of the single conducting layer, the metal spacers extending along the sidewalls of the dielectric layer.

Claim 13 is further allowable as Liu fails to teach wherein the dielectric layer comprises a low dielectric constant material.

Claim 14 is further allowable as Liu fails to teach wherein the dielectric layer is fluorine-doped silicon oxide.

Claim 100 is further allowable as Liu fails to teach wherein said dielectric layer extends completely underneath said conductive line.

Anticipation Rejection Based on U.S. Patent No. 6,197,682 to Drynan et al.

Claims 16 through 28, 101, and 116 through 129 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Drynan et al. (U.S. Patent No. 6,197,682). Applicant respectfully traverses this rejection, as hereinafter set forth.

Drynan teaches a structure of a contact hole in a semiconductor device and method of manufacturing the same. The structure includes a substrate 101 with an overlying silicon dioxide dielectric film 102, an overlying silicon nitride layer 103, a first wiring layer 108ac surrounded by a first dielectric layer 112, silicon nitride spacers 116a defining a contact plug 117 within the first dielectric layer 112, a overlying silicon nitride layer 113, a second wiring layer 118ac surrounded by a second dielectric layer 122, an overlying silicon nitride layer 123 and spacers 136a adjacent a conductive film 125. A second contact plug 137 fills in the space defined by spacers 136a.

By way of contrast, claim 16, as proposed to be amended, recites a metallization structure for a semiconductor device, comprising a substrate having a metal layer extending over said substrate, said metal layer at least underlying a conductive line, said conductive line for transmitting a signal across said substrate; a dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer, said at least one sidewall of said aperture defining said conductive line; a metal spacer abutting at least one sidewall of said at least one sidewall of the aperture; and a conductive layer in contact with said metal spacer, said conductive layer substantially filling a remaining portion of the aperture.

Applicant respectfully submits that Drynan fails to teach a metal layer at least underlying a conductive line, said conductive line for transmitting a signal across said substrate. Instead, Drynan only discloses conductive plugs 117, 137. Further, Drynan fails to teach a conductive layer in contact with said metal layer, said conductive layer substantially filling a remaining portion of the aperture. Instead, Drynan teaches conductive film 125 enclosed by a silicon nitride spacer 136a

wherein the silicon nitride spacer contacts the contact plug 137. As Drynan fails to teach every limitation of the presently claimed invention, applicants respectfully submit that Drynan fails to anticipate claim 16 of the presently claimed invention. Thus, independent claim 16 is allowable.

Claims 17 through 28 and 101 are each allowable as depending, either directly or indirectly, from independent claim 16.

Claim 27 is further allowable as Drynan fails to teach a plurality of upper metal layers on the conducting layer.

Applicant respectfully submit that claim 116, as proposed to be amended, is allowable for substantially the same reasons as claim 16. Claim 116, as proposed to be amended, recites a structure for transmitting a signal laterally across a substrate of a semiconductor device, said structure comprising a substrate having a metal layer of a conductive line disposed thereon; a dielectric layer above said metal layer, said dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer, said aperture at least extending a length of said conductive line; a metal spacer flanking at least one sidewall of said at least one sidewall of the aperture; and a conductive layer in contact with said metal spacer, said conductive layer substantially filling a remaining portion of the aperture.

Applicant respectfully submits that Drynan fails to teach a structure for transmitting a signal laterally across a substrate of a semiconductor device, said structure comprising a substrate having a metal layer of a conductive line disposed thereon. Instead, Drynan only discloses conductive plugs 117, 137. Further, Drynan fails to teach a conductive layer in contact with said metal layer, said conductive layer substantially filling a remaining portion of the aperture. Instead, Drynan teaches conductive film 125 enclosed by a silicon nitride spacer 136a wherein the silicon nitride spacer contacts the contact plug 137. As Drynan fails to teach every limitation of the presently claimed invention, applicants respectfully submit that Drynan fails to anticipate claim 116 of the presently claimed invention. Thus, independent claim 116 is allowable.

Claims 117 through 129 are each allowable as depending, either directly or indirectly, from allowable claim 116.

Claim 119 is further allowable as Drynan fails to teach a plurality of upper metal layers on the conducting layer.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 6,277,745 to Liu et al. in view of U.S. Patent No. 6,166,439 to Cox

Claims 2, 3, 100, 102 through 113, and 115 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Liu et al. (U.S. Patent No. 6,277,745) in view of Cox (U.S. Patent No. 6,166,439). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The discussion of Liu, above, is incorporated herein by reference. Cox discloses a low dielectric constant material and method of application to isolate conductive lines. Cox discloses a semiconductor device which includes a substrate and a conductive pattern formed on the substrate. The conductive pattern includes at least two conductive lines adjacent one another. A low dielectric constant material is disposed between the at least two conductive lines.

With respect to claims 2, 3, and 100, the Court of Appeals for the Federal Circuit has stated that "dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious." In re Fine, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). See also MPEP § 2143.03. Having failed to teach or suggest each and every limitation of claim 1 as proposed to be

amended, the prior art referenced as obviating dependent claims 2, 3 and 100, cannot serve as a basis for rejection.

By way of contrast with the proposed combination of references, claim 102, as proposed to be amended, recites a structure for transmitting a signal across a semiconductor device, said structure comprising a substrate comprising a substantially planar upper surface; and a conductive line extending over said upper surface and isolated therefrom by a dielectric layer at least underlying said conductive line, said conductive line comprising: a metal layer above said dielectric layer, said metal layer defining a pattern on a portion of the substrate upper surface; a single conducting layer overlying and substantially coextensive with the metal layer, said metal layer and said single conducting layer having substantially aligned sidewalls, wherein an upper surface of said single conductive layer is out of contact with any metal; and metal spacers flanking the sidewalls of the single conducting layer and metal layer.

Applicant respectfully submits that Liu fails to teach or suggest a single conducting layer having an upper surface that it out of contact with any metal. Applicants respectfully submit that no motivation exists, in either of the cited references, to remove the encapsulating layer in Liu because Liu teaches that a novel aspect of its invention are the fully encapsulated copper lines that are highly resistant to oxidation which is an otherwise inherent problem with bare copper lines. (Liu, abstract). However, in claim 102, as proposed to be amended, the conducting layer is out of contact with any metal. As the proposed combination fails to teach or suggest every limitation of independent claim 102, as proposed to be amended, and as no motivation exists to modify the cited references to include every limitation of independent claim 102, as proposed to be amended, applicant respectfully submits that claim 102 as proposed to be amended is not obvious in light of the proposed combination of Liu and Cox. Thus, claim 102 is allowable.

Claims 103 through 115 are each allowable as depending, either directly or indirectly, from allowable claim 102.

Claim 109 is further allowable as the proposed combination fails to teach or suggest the single conducting layer is an aluminum-copper alloy.

Claim 112 is further allowable as the proposed combination fails to teach or suggest a dielectric layer on the single conducting layer and having sidewalls aligned with said sidewalls of the single conducting layer, the metal spacers extending along the sidewalls of the dielectric layer.

Claim 114 is further allowable as the proposed combination fails to teach or suggest the dielectric layer is fluorine-doped silicon oxide.

Obviousness Rejection Based on U.S. Patent No. 6,277,745 to Liu et al.

Claim 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Liu et al. (U.S. Patent No. 6,277,745). Applicant respectfully traverses this rejection, as hereinafter set forth.

The Court of Appeals for the Federal Circuit has stated that "dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious." In re Fine, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). See also MPEP § 2143.03. Having failed to teach or suggest each and every limitation of claim 1 as proposed to be amended, the prior art referenced as obviating dependent claim 9, cannot serve as a basis for rejection.

Obviousness Rejection Based on U.S. Patent No. 6,277,745 to Liu et al. in view of U.S. Patent No. 6,046,502 to Matsuno

Claim 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Liu et al. (U.S. Patent No. 6,277,745) in view of Matsuno (U.S. Patent No. 6,046,502). Applicant respectfully traverses this rejection, as hereinafter set forth.

The Liu reference is discussed above and incorporated herein. Matsuno is directed toward a semiconductor device with improved adhesion between a titanium-based metal layer and an insulation film and fails to cure the deficiencies of Liu. Further, the Court of Appeals for the Federal Circuit has stated that "dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious." In re Fine, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). See

also MPEP § 2143.03. Having failed to teach or suggest each and every limitation of claim 1 as proposed to be amended, the prior art referenced as obviating dependent claim 14, cannot serve as a basis for rejection.

Obviousness Rejection Based on U.S. Patent No. 6,277,745 to Liu et al. in view of U.S. Patent No. 6,166,439 to Cox, and further in view of U.S. Patent No. 6,046,502 to Matsuno

Claim 114 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Liu et al. (U.S. Patent No. 6,277,745) in view of Cox (U.S. Patent No. 6,166,439), and further in view of Matsuno (U.S. Patent No. 6,046,502). Applicant respectfully traverses this rejection, as hereinafter set forth.

The Liu reference is discussed above and incorporated herein. Matsuno is directed toward a semiconductor device with improved adhesion between a titanium-based metal layer and an insulation film and fails to cure the deficiencies of Liu. Further, the Court of Appeals for the Federal Circuit has stated that "dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious." In re Fine, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). See also MPEP § 2143.03. Having failed to teach or suggest each and every limitation of claim 102 as proposed to be amended, the prior art referenced as obviating dependent claim 114, cannot serve as a basis for rejection.

ENTRY OF AMENDMENTS

The proposed amendments to claims 1, 8, 9, 12, 16, 102, 108, 109, 112 and 116 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, the amendments do not raise new issues or require a further search. Finally, if the Examiner determines that the amendments do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 1 through 28 and 100 through 129 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully Submitted,

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KWP/hlg:dlm
Enclosure: Version With Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Twice amended) A metallization structure for a semiconductor device, comprising:
a substrate comprising a substantially planar upper surface; and
a conductive line for transmitting a signal laterally across said substrate, said conductive line comprising:
a metal layer defining a pattern on a portion of the substrate upper surface;
a single conducting layer overlying and substantially coextensive with the metal layer, said metal layer and said single conducting layer having substantially aligned sidewalls and an upper surface out of contact with any metal; and
metal spacers flanking the sidewalls of the single conducting layer and metal layer.

8. (Amended) The metallization structure of claim 1, wherein the single conducting layer is selected from the group comprising aluminum and copper.

9. (Amended) The metallization structure of claim 8, wherein the single conducting layer is an aluminum-copper alloy.

12. (Twice amended) The metallization structure of claim 1, further comprising a dielectric layer on the conducting layer and having sidewalls aligned with said sidewalls of the single conducting layer, the metal spacers extending along the sidewalls of the dielectric layer.

16. (Twice amended) A metallization structure for a semiconductor device, comprising:
a substrate having a metal layer extending over said substrate, said metal layer at least underlying a conductive line, said conductive line for transmitting a signal across said substrate;

a dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer, said at least one sidewall of said aperture [flanking] defining said conductive line;

a metal spacer abutting at least one sidewall of said at least one sidewall of the aperture; and

a conductive layer in contact with said metal spacer, said conductive layer substantially filling a remaining portion of the aperture.

102. (Amended) A structure for transmitting a signal across a semiconductor device, said structure comprising:

a substrate comprising a substantially planar upper surface; and

a conductive line extending over said upper surface and isolated therefrom by a dielectric layer at least underlying said conductive line, said conductive line comprising:

a metal layer above said dielectric layer, said metal layer defining a pattern on a portion of the substrate upper surface;

a single conducting layer overlying and substantially coextensive with the metal layer, said metal layer and said single conducting layer having substantially aligned sidewalls, wherein an upper surface of said single conductive layer is out of contact with any metal; and

metal spacers flanking the sidewalls of the single conducting layer and metal layer.

108. (Amended) The structure of claim 102, wherein the single conducting layer is selected from the group comprising aluminum and copper.

109. (Amended) The structure of claim 108, wherein the single conducting layer is an aluminum-copper alloy.

112. (Amended) The structure of claim 102, further comprising a dielectric layer on the single conducting layer and having sidewalls aligned with said sidewalls of the single conducting layer, the metal spacers extending along the sidewalls of the dielectric layer.

116. (Amended) A structure for transmitting a signal laterally across a substrate of a semiconductor device, said structure comprising:

a substrate having a metal layer of a conductive line disposed thereon;

a dielectric layer above said metal layer, said dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer, said aperture at least extending a length of said conductive line;

a metal spacer flanking at least one sidewall of said at least one sidewall of the aperture; and

a conductive layer in contact with said metal spacer, said conductive layer substantially filling a remaining portion of the aperture.